Jonathan Barnes

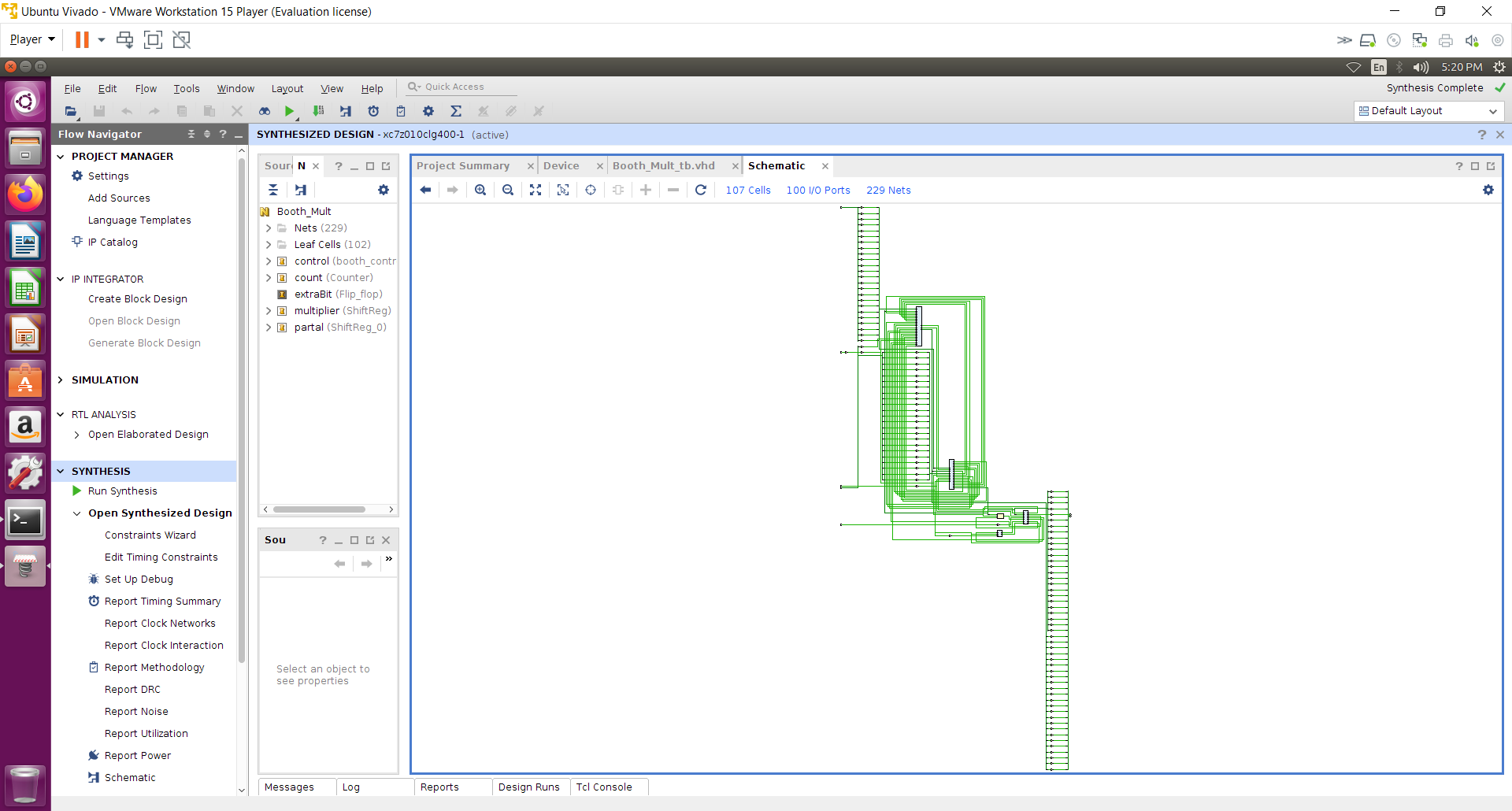
Project 2 report

**Design Summary:**

For this project I reused the CLA that I designed for the previous project. I used the CLA because it was faster than the ripple carry adder. I designed the FSM (finite state machine) that would be controlling the multiplier, through control signals. The FSM has two processes one that is triggered by the clock and updates the state of the multiplier, and the other which is combinational, and changes the output signals, and sets the next state. I then designed the counter, the counter is supposed to count the number of times the multiplier shifts right from 0 to 23. The counter process is triggered by the shift signal going high, and it uses my previously implemented CLA for the addition. After that I implemented the shift registers. The shift registers will receive signals that tell them to clear all bits, shift bits by one to the right, or load in all new bits in parallel. The parallel in and shift in will be provided as inputs. I also implemented a flip flop as a register for an extra bit, it also receives a clear, and shift signal. Finally I worked on the top level implementation for the multiplier. This I implemented with combinational logic, just wiring signals between the different parts, and a little Boolean algebra to decide if the partial product register needed to be loaded or not.

You can see the generated schematics below.

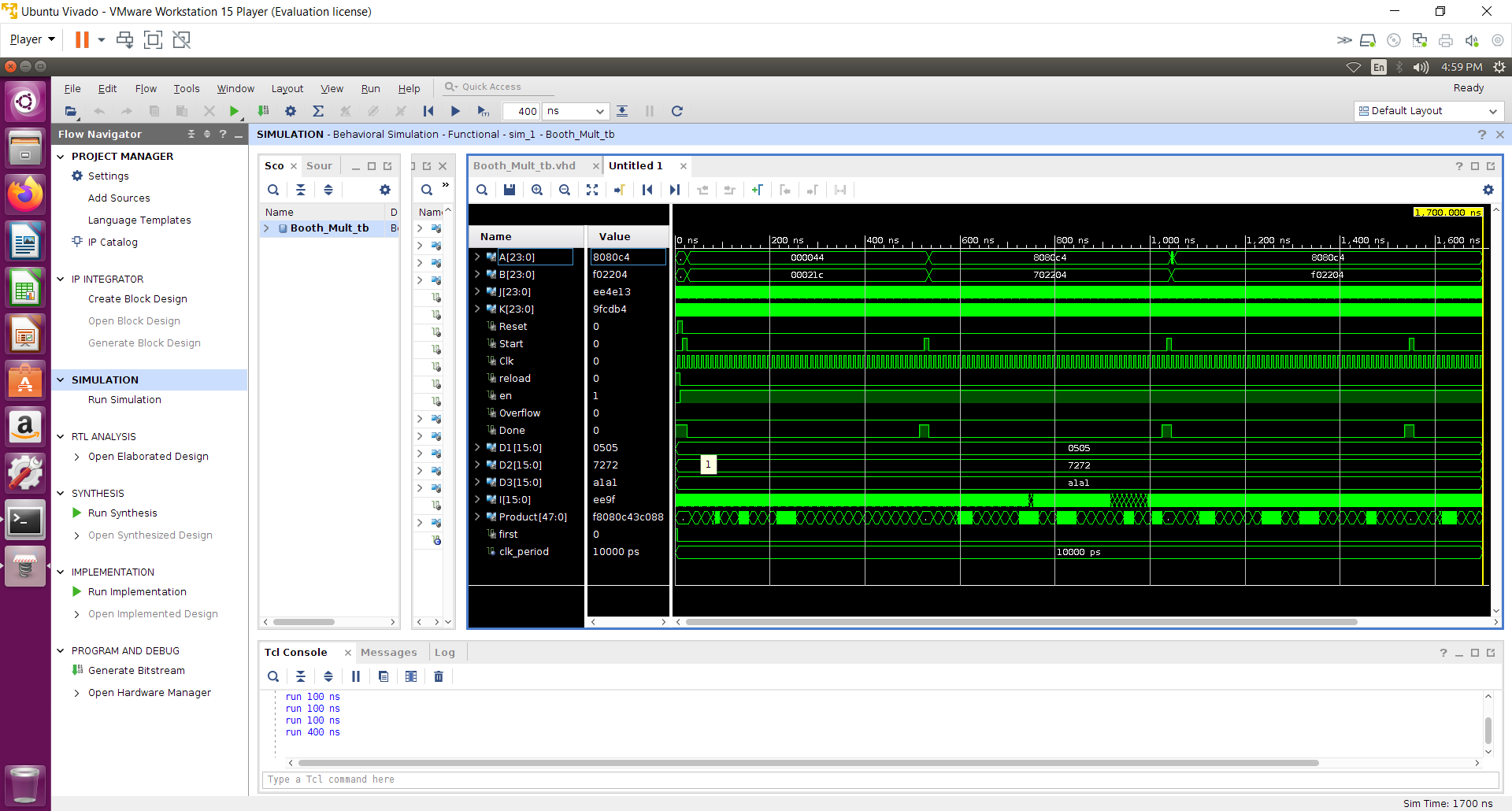
**Booth Mult:**



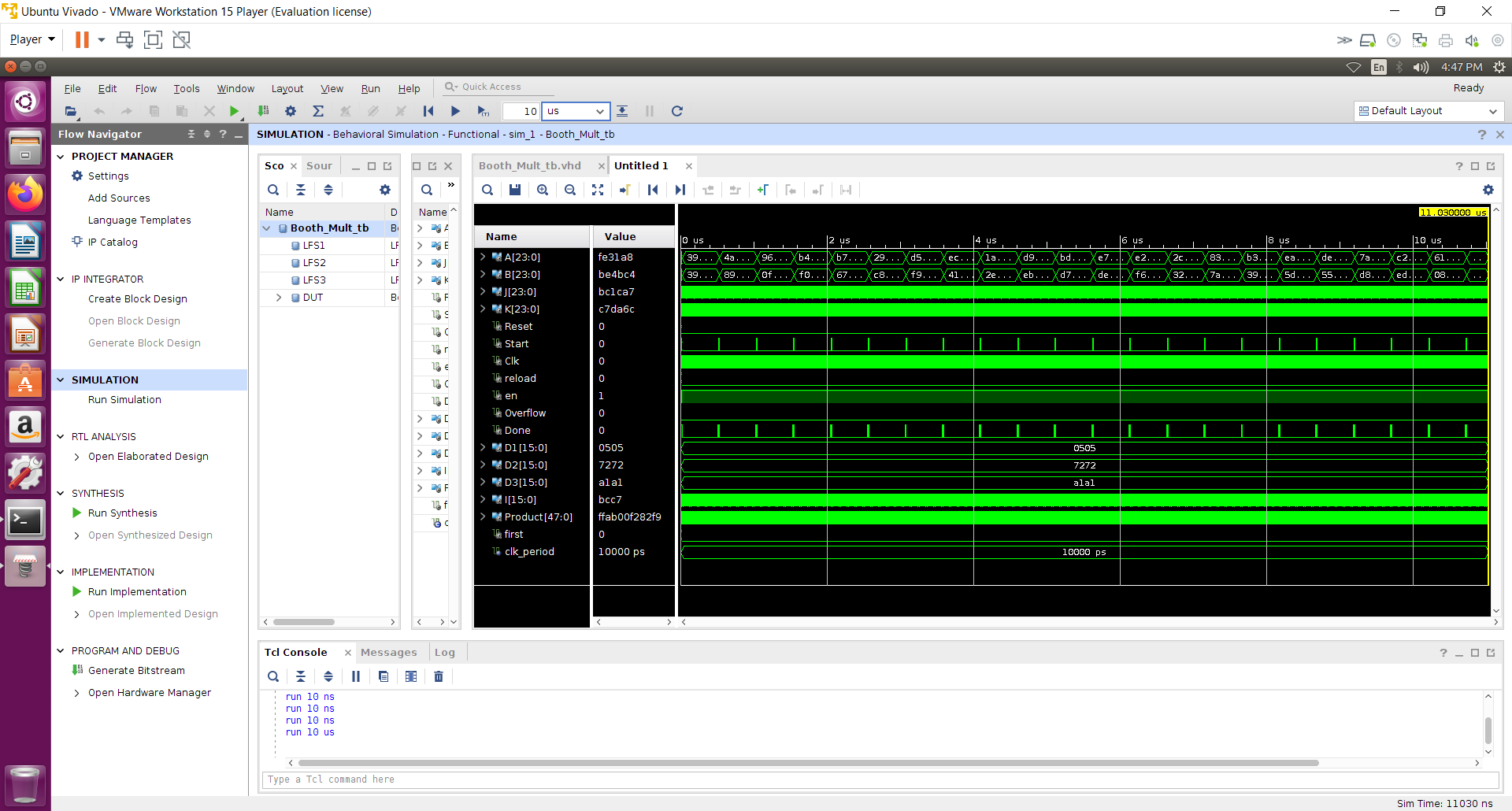
**Design simulation results:**

To test my designs I first used pre-set stable values for A and B. And for my second test I utilized 4 instantiations of LFSR’s to generate pseudo random inputs to A and B. In creating the Test bench I used 4 processes, one was the clock, another seeded the LFSR’s and enabled them, the third controlled the start signal, and the inputs A and B, and the final process was for assert statements to check for correctness. To check for correctness I just stepped forward on the waveform till I saw the done signal and checked if there was an error printed to the console. I repeated this step several times until I was convinced there were no errors. You can see waveforms below.

**Stable:**



**Unstable:**



**Design Implementation Report:**

1. Hardware utilization

|  |  |
| --- | --- |
| Booth Mult in wrapper |  |
| LUT | 152 |
| IO | 77 |
| FF | 175 |
| BUFG | 2 |

1. Power

Dynamic power = .013W 13%

* Sig 9%
* Logic 4%
* IO 63%
* Clocks 24%

Static power = .093W 87%

1. Timing report

clock period = 4 ns

WNS = -0.543 ns

Critical path = 4.543 ns

1. Design Schematic can be seen in design summary section